This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented): An amplifier formed on a silicon substrate, comprising:

first and second differential legs, each driving first and second resistive loads;

said first resistive load comprising first and second parallel resistive loads connected on one side thereof to one end of said first differential leg and the other side of each of said first and second parallel resistive loads separately connected to a first reference voltage;

said second resistive load comprising third and fourth resistive loads each connected on one side thereof to one end of said second differential leg and the other side of each of said third and fourth parallel resistive loads connected separately to said first reference voltage;

each of said first, second, third and fourth resistive loads fabricated of a strip of resistive material disposed on the surface of the substrate and having a finite resistivity, length, width and thickness;

said first parallel resistive load disposed adjacent to a first dummy resistive strip on one side thereof and capacitively coupled thereto, and disposed adjacent said third parallel resistive load on the opposite side thereof and capacitively coupled thereto;

said third parallel resistive load disposed adjacent a second dummy resistive strip disposed on the diametrically opposite side thereof from said first parallel resistive load and capacitively coupled thereto;

said fourth parallel resistive load disposed adjacent said second dummy resistive strip and capacitively coupled thereto on the diametrically opposite side thereof from said third parallel resistive load;

said second resistive load disposed adjacent said fourth parallel resistive load on the side diametrically opposite to said second dummy resistive strip and capacitively coupled thereto;

said second parallel resistive load disposed adjacent a third dummy resistive strip on the side thereof diametrically opposite to said second parallel resistive load and capacitively coupled thereto; and

said first, second and third dummy resistive strips connected to a second reference voltage.

2. (Previously Presented): The amplifier of Claim 1, wherein said first reference voltage and said second reference voltage are common.

3. (Currently Amended): The amplifier of Claim 2, wherein said first reference voltage and said ~~first~~ second reference voltage comprise ground.

4.(Previously Presented): The method of Claim 1, wherein each of said first, second, third and fourth resistive loads have substantially equal resistance.

5. (Previously Presented): The amplifier of Claim 4, wherein each of said first, second, third and fourth resistive loads have a dimension substantially equal to each other.

6. (Previously Presented): The amplifier of Claim 5, wherein each of said first, second, third and fourth resistive loads are disposed on the silicon substrate in a parallel manner, such that one edge of each of the first, second, third and fourth parallel resistive loads are parallel to each other.

7. (Previously Presented): The amplifier of Claim 6, wherein said first, second and third dummy resistive strips are substantially identical to said first, second, third and fourth parallel resistive loads.

8. (Previously Presented): The amplifier of Claim 1, wherein said resistive material comprises polycrystalline silicon disposed on the surface of the substrate and separated therefrom by an insulator.

9. (Previously Presented): The amplifier of Claim 1, wherein said strips of resistive material from which said first, second, third and fourth parallel resistive loads are formed are formed of a rectangular strip of resistive material and the longest edges thereof parallel to each other.

10. (Currently Amended): The amplifier of Claim 9, wherein each of said first, second and third dummy resistor strips are formed of a rectangular strip of resistive material and are substantially parallel to each of said first, second, third and fourth parallel resistive loads.

11. (Previously Presented): The amplifier of Claim 1, wherein each of said first, second, third and fourth parallel resistive loads is capacitively coupled to either another of said first, second, third and fourth parallel resistive loads or one of said first, second and third dummy resistor strips by a distributed capacitance.